WHAT IS CLAIMED IS:

1. A control chip with a bus cycle inhibiting function for preventing internal bus cycle type of the control chip, picked up from a first bus, from being re-transmitting to a second bus of the control chip, the control chip comprising:

a bus cycle inhibiting circuit for receiving a bus cycle from the first bus and outputting an inhibiting signal once the bus cycle is determined to be an internal bus cycle type of the control chip; and

a bus bridging circuit coupled to the bus cycle inhibiting circuit for inhibiting the re-transmission of the bus cycle on receiving the inhibiting signal.

2. The control chip of claim 1, wherein the bus cycle inhibiting circuit comprises:

a bus resource decode circuit for receiving a bus cycle from the first bus and outputting an indicator signal representing the particular type of bus cycle when the bus cycle is determined to be an internal bus cycle type of the control chip; and

a logic circuit for outputting the inhibiting signal according to a preset enable value and the indicator signal.

3. The control chip of claim 2, wherein the bus resource decode circuit comprises:

an input/output resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal input/output bus cycle when the bus cycle is determined to be an internal input/output bus cycle;

a memory resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal memory bus cycle when the bus cycle is determined to be an internal memory bus cycle; and

a configuration resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal configuration bus cycle when the bus cycle is determined to be an internal configuration bus cycle.

4. The control chip of claim 2, wherein the logic circuit comprises AND gates and OR gates.

5. The control chip of claim 2, wherein the preset enable value is stored inside a register.

6. The control chip of claim 1, wherein the second bus comprises a peripheral component interconnect (PCI) bus.

7. The control chip of claim 1, wherein the control chip comprises a South-bridge control chip.

8. A bus cycle inhibiting circuit for a control chip having at least a first bus and a second bus, comprising:

a bus resource decode circuit for receiving a bus cycle from the first bus and outputting an indicator signal representing the particular type of bus cycle when the bus cycle is determined to be an internal bus cycle; and

a logic circuit for outputting the inhibiting signal according to a preset enable value and the indicator signal.

9. The bus cycle inhibiting circuit of claim 8, wherein the bus resource decode circuit comprises:

an input/output resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal input/output bus cycle when the bus cycle is determined to be an internal input/output bus cycle;

a memory resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal memory bus cycle when the bus cycle is determined to be an internal memory bus cycle; and

a configuration resource decode unit for receiving a bus cycle from the first bus and outputting an indicator signal representing an internal configuration bus cycle when the bus cycle is determined to be an internal configuration bus cycle.

10. The bus cycle inhibiting circuit of claim 8, wherein the logic circuit furthermore comprises AND gates and OR gates.

11. The bus cycle inhibiting circuit of claim 8, wherein the preset enable value is stored inside a register.

12. The bus cycle inhibiting circuit of claim 8, wherein the second bus comprises a peripheral component interconnect (PCI) bus.

13. The bus cycle inhibiting circuit of claim 8, wherein the control chip comprises a South-bridge control chip.

14. A method of inhibiting the bus cycles of a control chip having at least a first bus and a second bus, comprising:

receiving a bus cycle from the first bus and determining if the bus cycle is an internal bus cycle type of the control chip, and outputting an inhibiting signal if the bus cycle is an internal bus cycle type of the control chip; and

inhibiting the re-transmission of the bus cycle to the second bus according to the actual state of the inhibiting signal.

15. The bus cycle inhibiting method of claim 14, wherein the inhibiting signal is issued when the bus cycle is found to be an internal input/output bus cycle, an internal memory bus cycle or an internal configuration bus cycle.

16. The bus cycle inhibiting method of claim 15, wherein a preset enable value is also referenced before issuing the inhibiting signal.

17. The bus cycle inhibiting method of claim 14, wherein the second bus comprises a peripheral component interconnect (PCI) bus.

18. The bus cycle inhibiting method of claim 14, wherein the control chip comprises a South-bridge control chip.